I Claim:

1. Apparatus for testing an integrated circuit on a wafer, comprising:

a) a test circuit formed on the wafer with the integrated circuit, the test circuit comprising:

i) a ring oscillator circuit:

II) a plurality of sub-circuits coupled to the ring oscillator circuit;

iii) a control circuit to selectively couple the sub-circuits to the ring oscillator circuit, and

b) a test unit separate from the wafer, the test unit linked to the test circuit to transmit a signal to activate the test circuit,

wherein the test circuit when activated by the test unit conducts a separate test of the integrated circuit for each sub-circuit selected by the control circuit.

2. The apparatus of claim 1 wherein each test conducted by the test circuit is a parametric test.

3. The apparatus of claim 2 wherein the sub-circuits when coupled to the ring oscillator circuit change the frequency of oscillation of the ring oscillator circuit.

4. The apparatus of claim 3 wherein at least one sub-circuit comprises a capacitive load to change the frequency of oscillation of the ring oscillator circuit.

5. The apparatus of claim 3 wherein at least one sub-circuit comprises a capacitive load and a resistive load to change the frequency of oscillation of the ring oscillator circuit.

6. The apparatus of claim 3 wherein at least one sub-circuit comprises a delay element to change the frequency of oscillation of the ring oscillator circuit.

7. The apparatus of claim 4 wherein the capacitive load comprises at least one capacitor.

8. The apparatus of claim 5 wherein the capacitive load comprises at least one capacitor and the resistive load comprises at least one resistor.

9. The apparatus of claim 6 wherein the delay element comprises at least one inverter.

10. The apparatus of claim 9 wherein each inverter is a standard CMOS inverter.

11. The apparatus of claim 1 wherein the control circuit comprises a sequencer to selectively couple the sub-circuits to the ring oscillator circuit to produce a series of test states.

12. The apparatus of claim 1 wherein the signal produced by the test unit is a power signal sufficient to energize the test circuit.

13. The apparatus of claim 1 wherein the test circuit is formed on the wafer with at least two metallization layers of the integrated circuit.

14. The apparatus of claim 1 wherein the test circuit is formed on the wafer with at least one metallization layer and one polysilicon layer of the integrated circuit.

15. The apparatus of claim 2 wherein the test circuit further comprises a transmitter circuit to transmit a test result signal from the test circuit to the test unit.

16. The apparatus of claim 15 wherein said test unit comprises a receiver circuit to receive the test result signal from the test circuit.

17. The apparatus of claim 16 wherein the test unit further comprises a circuit to analyze and display the test result signal.

18. The apparatus of claim 17 wherein the analyzing circuit calculates a value of the parameter being tested.

19. The apparatus of claim 18 wherein the analyzing circuit calculates a ratio of the values of the parameters being tested.

20. The apparatus of claim 19 wherein the test result signal is the output of the ring oscillator circuit.

21. The apparatus of claim 11 wherein the test circuit further comprises an antenna adapted to receive the signal from the test unit and a power supply circuit coupled to the antenna and adapted to provide power to the test circuit.

22. The apparatus of claim 21, wherein the power supply circuit comprises a voltage rectifier coupled to the antenna, a voltage regulator coupled to the voltage rectifier and an energy storage element coupled to the voltage regulator, wherein the power supply circuit is adapted to provide a plurality of voltage levels to the test circuit.

23. The apparatus of claim 21, wherein the control circuit further comprises a second ring oscillator adapted to provide a first clock signal, and a divider coupled to the second ring oscillator and the sequencer and adapted to provide a second clock signal, wherein the second clock signal is provided to the sequencer so that the sequencer can provide a series of test state signals to the ring oscillator and plurality of sub-circuits.

24. The apparatus of claim 15, wherein the transmitter circuit comprises a coupler which is coupled to the ring oscillator and an antenna and is adapted to selectively couple the output of the ring oscillator to the antenna for transmission of the test result signal to the test unit.

25. The apparatus of claim 24 wherein the coupler capacitively couples the test result signal to the antenna.

26. The apparatus of claim 24 wherein the coupler modulates the impedance of the antenna to transmit the test result signal to the test unit.

27. The apparatus of claim 12 wherein the power signal produced by the test unit is a RF power signal.

28. The apparatus of claim 1 wherein there are a plurality of test circuits on the wafer and the test unit tests each test circuit sequentially.

29. The apparatus of claim 1 wherein there is a plurality of test circuits on the wafer and the test unit tests the plurality of test circuits in parallel.

30. The apparatus of claim 1, wherein the test circuit is formed adjacent to a die containing the integrated circuit.

31. The apparatus of claim 1 wherein the test circuit is formed on a die that contains the integrated circuit.

32. The apparatus of claim 1 wherein said test circuit is formed on a large percentage of dies on the wafer.

33. The apparatus of claim 1 wherein said test circuit is formed on dies near the edge of said wafer.

34. A test circuit for testing an integrated circuit on a wafer, the test circuit formed on the wafer with the integrated circuit, the test circuit comprising:

a) a ring oscillator circuit;

b) a plurality of sub-circuits coupled to the ring oscillator circuit; and

c) a control circuit to selectively couple the sub-circuits to the ring oscillator circuit,

wherein the test circuit conducts a separate test of the integrated circuit for each sub-circuit selected by the control circuit.

35. The test circuit of claim 34 wherein each test conducted by the test circuit is a parametric test.

36. The test circuit of claim 35 wherein the sub-circuits when coupled to the ring oscillator circuit change the frequency of oscillation of the ring oscillator circuit.

37. The test circuit of claim 36 wherein at least one sub-circuit comprises a capacitive load to change the frequency of oscillation of the ring oscillator circuit.

38. The test circuit of claim 37 wherein at least one sub-circuit comprises a capacitive load and a resistive load to change the frequency of oscillation of the ring oscillator circuit.

39. The test circuit of claim 38 wherein at least one sub-circuit comprises a delay element to change the frequency of oscillation of the ring oscillator circuit.

40. The test circuit of claim 37 wherein the capacitive load comprises at least one capacitor.

41. The test circuit of claim 38 wherein the capacitive load comprises at least one capacitor and the resistive load comprises at least one resistor.

42. The test circuit of claim 39 wherein the delay element comprises at least one inverter.

43. The test circuit of claim 42 wherein each inverter is a standard CMOS inverter.

44. The test circuit of claim 34 wherein the control circuit comprises a sequencer to selectively couple the sub-circuits to the ring oscillator circuit to produce a series of test states.

45. The test circuit of claim 34 wherein the test circuit is formed on the wafer with at least two metallization layers of the integrated circuit.

46. The apparatus of claim 34 wherein the test circuit is formed on the wafer with at least one metallization layer and one polysilicon layer of the integrated circuit.

47. The test circuit of claim 34 wherein the test circuit produces a test result signal that is the output of the ring oscillator circuit.

48. The apparatus of claim 44 wherein the test circuit further comprises an antenna adapted to receive a signal, a power supply circuit coupled to the antenna and adapted to provide power to the test circuit and a transmitter circuit coupled to the ring oscillator and the antenna and adapted to transmit a test result signal.

49. The apparatus of claim 48, wherein the power supply circuit comprises a voltage rectifier coupled to the antenna, a voltage regulator coupled to the voltage rectifier and an energy storage element coupled to the voltage regulator, wherein the power supply circuit is adapted to provide a plurality of voltage levels to the test circuit.

50. The apparatus of claim 48, wherein the control circuit further comprises a second ring oscillator adapted to provide a first clock signal, and a divider coupled to the second ring oscillator and the sequencer and adapted to provide a second clock signal, wherein the second clock signal is provided to the sequencer so that the sequencer can provide a series of test state signals to the ring oscillator and plurality of sub-circuits.

51. The apparatus of claim 48, wherein the transmitter circuit comprises a coupler which is coupled to the ring oscillator and the antenna and is adapted to selectively couple the output of the ring oscillator to the antenna for transmission of the test result signal.

52. The test circuit of claim 51 wherein the coupler capacitively couples the test result signal to the antenna.

53. The test circuit of claim 51 wherein the coupler modulates the impedance of the antenna to transmit the test result signal.

54. The test circuit of claim 34 wherein the test circuit is formed adjacent to a die containing the integrated circuit.

55. The test circuit of claim 34 wherein the test circuit is formed on a die that contains the integrated circuit.

56. The test circuit of claim 34 wherein the test circuit is formed on a large percentage of dies on the wafer.

57. The test circuit of claim 34 wherein the test circuit is formed on dies near the edge of the wafer.

58. A method of testing an integrated circuit on a wafer using a test circuit formed on the wafer with the integrated circuit, the test circuit comprising a ring oscillator circuit, a plurality of sub-circuits coupled to the ring oscillator circuit wherein each sub-circuit changes the frequency of oscillation of the ring oscillator circuit, and a control circuit to selectively couple the sub-circuits to the ring oscillator circuit, the method comprising:

(a) activating the test circuit;

(b) sequentially coupling the sub-circuits to the ring oscillator circuit to selectively change the frequency of oscillation of the ring oscillator circuit;

(c) producing a test result signal in response to each sub-circuit selected by the control circuit; and,

(d) analyzing the test result signal to determine the frequency of oscillation.

59. The method of claim 58, wherein each test conducted by the test circuit is a parametric test.

60. The method of claim 59, wherein step (d) of the method further comprises:

(e) calculating a value for the parameter being tested.

61. The method of claim 59, wherein step (d) of the method further comprises:

(f) calculating a ratio of values for the parameter being tested.

62. The method of claim 58, wherein step (b) further comprises the steps of:

(g) providing a clock signal; and,

(h) generating a sequence of test states and state signals based on the clock signal to switchably couple the sub-circuits to the variable ring oscillator.

63. The method of claim 62, wherein step (d) further comprises the steps of:

(i) coupling the test result signal to an antenna within the test circuit through a coupler in the test circuit; and,

(j) enabling and disabling the coupler to intermittently transmit the test result signal to a test unit to allow the test unit to synchronize to the test result signal and analyze the test result signal.

64. The method of claim 58, wherein at least one sub-circuit comprises a capacitive load to change the frequency of operation of the ring oscillator circuit.

65. The method of claim 58, wherein at least one sub-circuit comprises a capacitive load and a resistive load to change the frequency of operation of the ring oscillator circuit.

66. The method of claim 58, wherein at least one sub-circuit comprises a delay element to change the frequency of oscillation of the ring oscillator circuit.

67. The method of claim 58, wherein the control circuit comprises a sequencer.

68. The method of claim 58, wherein there are a plurality of test circuits on the wafer and the method further comprises testing each test circuit sequentially.

69. The method of claim 58, wherein there are a plurality of test circuits on the wafer and the method further comprises test each test circuit in parallel.

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